PUN-ENCODED CM85A CIRCUIT SCHEMATICS OCCLUSION ARRAY ONLY

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BTC Hardware Models

- SCHEMATIC 23a: Occlusion Array (Dnet 21)
- SCHEMATIC 23b: Occlusion Array (Dnet 22)
- SCHEMATIC 23c: Occlusion Array (2-level Dnet)
- SCHEMATIC 23d: Occlusion Array (raw multilevel benchmark)
- SCHEMATIC 23e: Occlusion Array (clean multilevel benchmark)

S23a is an Occlusion Array, BTC's FPGA-like reconfigurable architecture. The circuit expressed within the array is **S6b**.

S23b is the Occlusion Array for **S7a**.

S23c is the Occlusion Array for **S1**.

S23d is the Occlusion Array for **S2**.

S23e is the Occlusion Array for **S2**, with some obvious redundancy removed and ordered cells

Although the array configuration is recognizably different for each of these five circuits, the functioning of the array is the same. Occlusion arrays process in almost constant time, regardless of array configuration. thus the design differences over these five circuits are irrelevant to the efficiency of the array operation. Bad design uses a larger array area (**S23d**), but does not effect either the timing or the wiring complexity, since Occlusion Arrays abstract both timing and wiring into spatial configurations of marked memory locations.

BTC Hardware Models

- SCHEMATIC 23a: Occlusion Array, optimized
  homogeneous hardware substrate, a modified memory
  optimized circuit expressed as a software array
  functionality of circuit is expressed in memory
  clocking and wiring are in the substrate not in the design
  marks in array represent and abstract wires
  nearly constant time performance
  performance largely independent of complexity of circuit
  different arrays correspond to different circuit structures

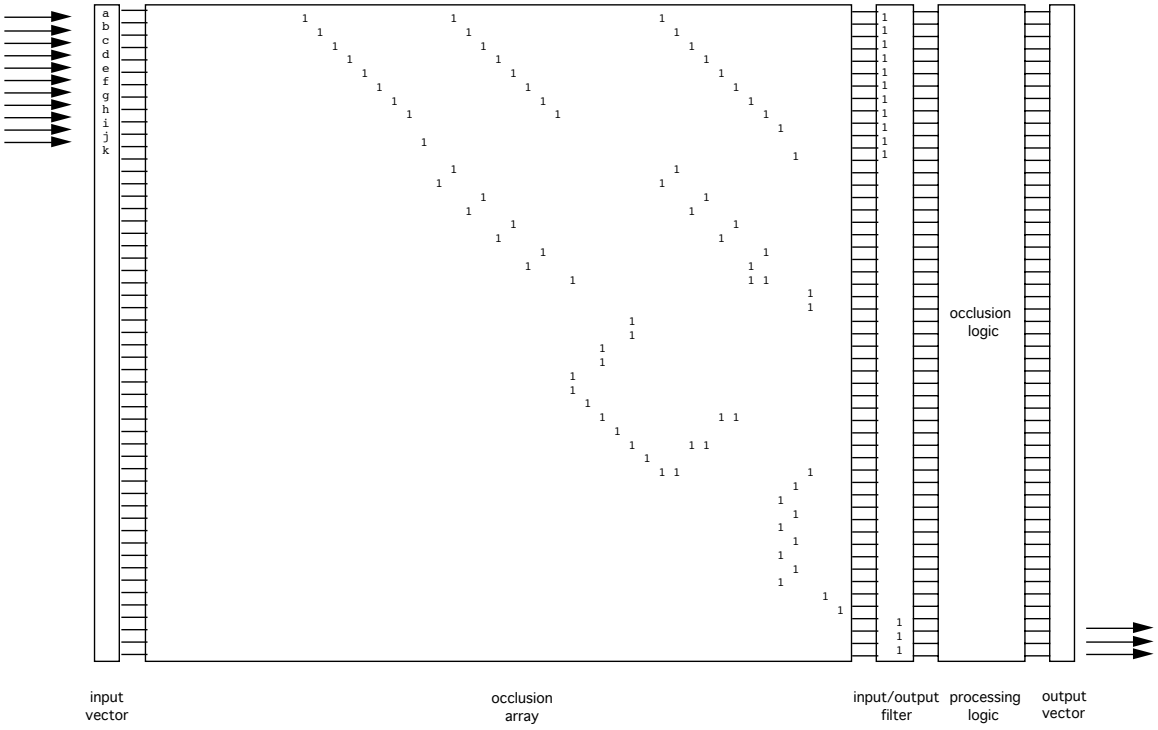
- SCHEMATIC 23b: Occlusion Array, testable
  homogeneous hardware substrate, a modified memory
  testable circuit expressed as a software array
  hardware testability is not a relevant concept
  identical performance to other arrays

- SCHEMATIC 23c: Occlusion Array, 2-level
  homogeneous hardware substrate, a modified memory
  2-level circuit expressed as a software array
  2-level shifts array marks to edges
  constant performance over all inputs guaranteed
  array empty space can be reclaimed, not wasted

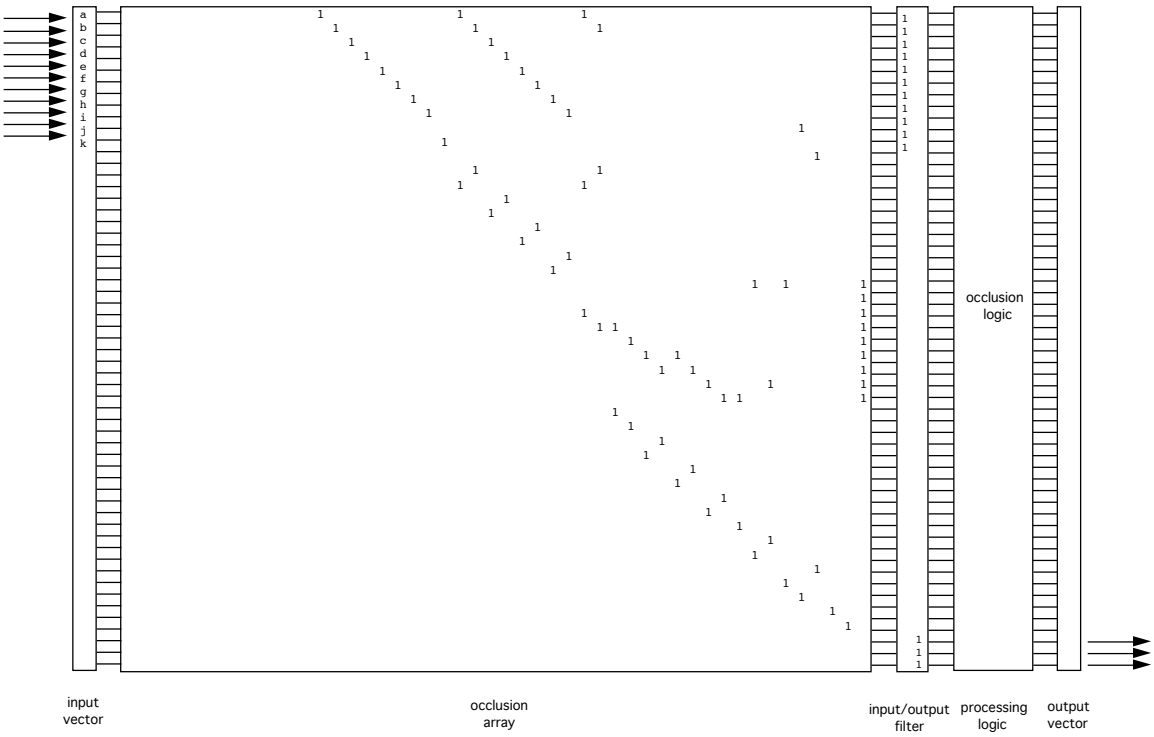
- SCHEMATIC 23d: Occlusion Array, benchmark
  homogeneous hardware substrate, a modified memory
  benchmark circuit expressed as a software array
  poor design and lack of optimization make array larger
  poor design does not effect processing time of array

- SCHEMATIC 23e: Occlusion Array, cleaned benchmark
  homogeneous hardware substrate, a modified memory
  benchmark circuit expressed as a software array
  poor design and lack of optimization make array larger
  poor design does not effect processing time of array
  design rows reorganized from 23d
  some obvious redundancy removed (two inverters in a row)

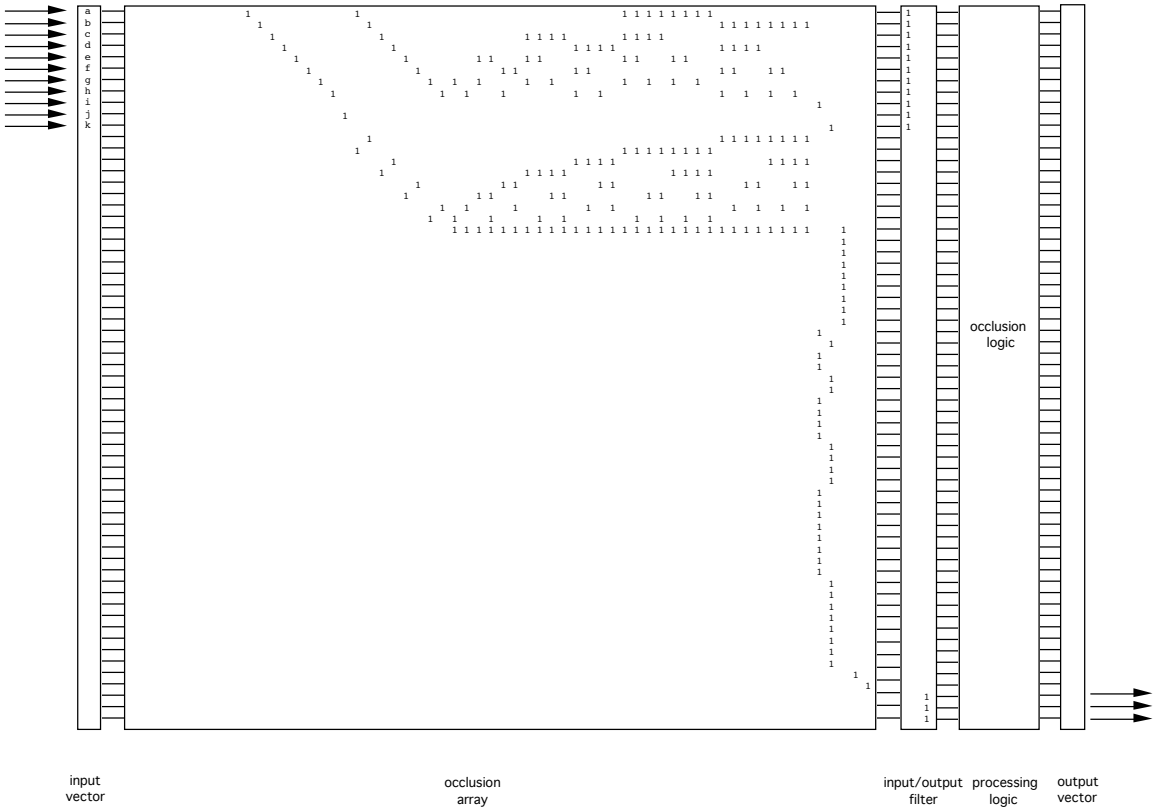
SCHEMATIC 23a: Occlusion Array (Dnet 21)



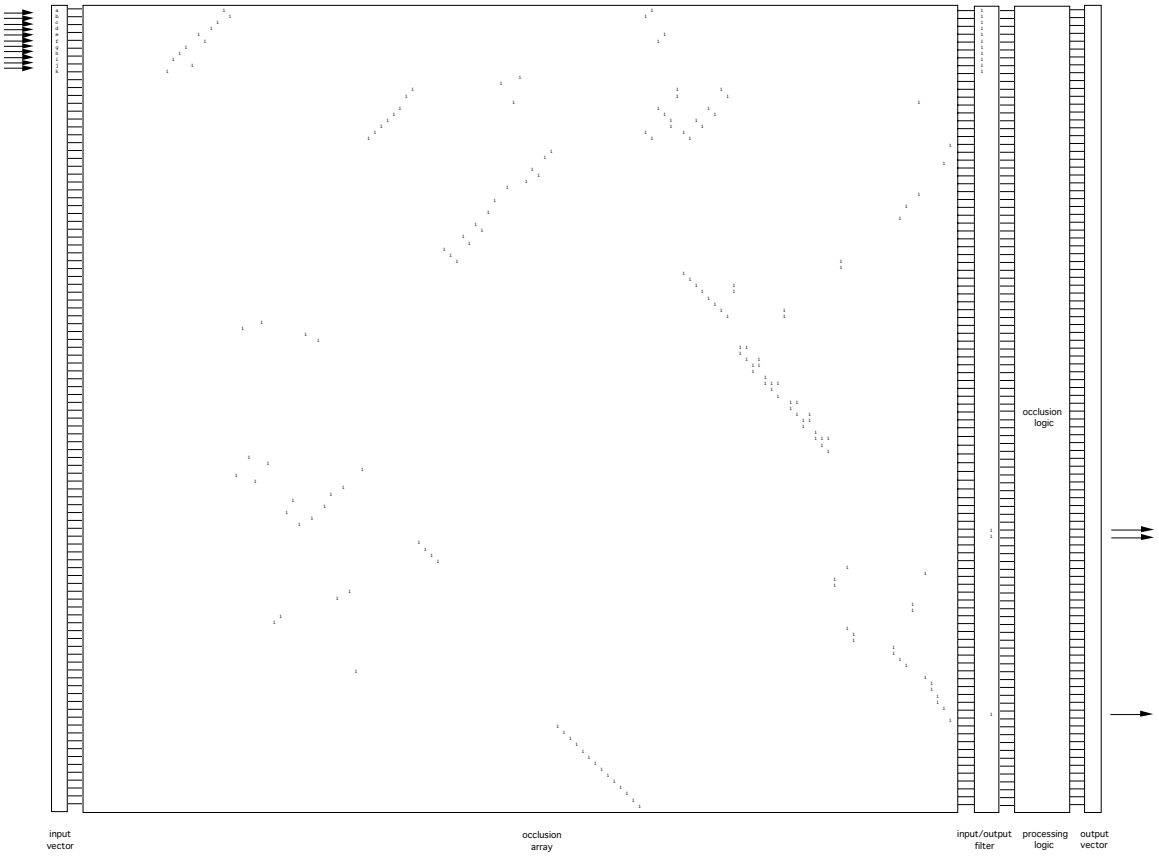
SCHEMATIC 23b: Occlusion Array (Dnet 22)



SCHEMATIC 23c: Occlusion Array (2-level Dnet)



SCHEMATIC 23d: Occlusion Array (raw multilevel benchmark)



SCHEMATIC 23e: Occlusion Array (clean multilevel benchmark)