FROM SKETCH TO SILICON

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[Note: Going from sketch to silicon is not really possible without the CoMesh hardware because 90% of design integration is timing, and for standard architectures that requires iterative convergent modeling/twiddling to get to pre-laying timing closure and the more of the same to get post-layout timing convergence. Design changes require complete reiteration of both pre and post timing. So this idea is "Visio for EDA" when put into the context of any FPGA architecture; that is it would be sketching with no functional simulation properties, a dubious win. The evolution of the idea, as well as the details of the technical realization, have CoMesh silicon at the base, cause then design without timing becomes possible.]

Scenario

Imagine two engineers sitting at dinner, talking over the potentials of their new project. They have to design a high-speed SERDES communications hub with dynamically reconfigurable routing to serve a dozen high volume clients. Each client will send minute-long bursts of hundreds of gigabits of video-on-demand data to be routed to half-a-dozen local communications hubs that will in turn send the data onto local customers. The engineers scratch their collective head, wondering how to get the router to be maximally responsive to a different high-volume client that changes every minute.

The trusty napkin is unfolded. "We know how to build the SERDES i/o channel," one says. A box is sketched on the napkin and labeled. A line goes into and out of this box. "We know how the distribution protocol might work." The other engineer draws a strike across the output line. "You know, we better have 64-bit output into the router." "64" gets written above the stroke. "But," says the first, "there's no FPGA that can handle that! What about 8 FPGAs and eight data-streams?" "Too expensive" is the immediate consensus. "Besides, how do we manage to get them to coordinate efficiently? Let's go with a CoMesh FPBA."

A box labeled CoMesh is drawn in the middle, connected to a smaller box labeled "output protocol". "Well, let's do this incrementally, we know the protocol." Several logic equations are scribbled down. "Here's the FSM that applies the protocols to the routing." Some FSM graphs appear on the napkin.

"The night is young, it's only 8pm, and my wife doesn't expect me back home until 10. Let's go back to the lab and run it in silicon."

Technology

The CoMesh Sketch™ interface permits designers to convert top-down design into a partially or fully functional silicon implementation directly, without HDL, without elaborate timing models, without the headache of post-layout timing convergence, literally without effort.

Sketch recognizes labeled function diagrams, bit-width notations, logic equations, FSMs, and HDL fragments. It matches recognized function boxes to its functional component library; it parametrically generates functions for any bit-width; it synthesizes abstract logical and FSM specifications into functional netlists; it integrates function blocks with connective logic; constructs abstract templates for not yet specified components; and it synthesizes the entire design into a seamless, highly optimized configuration file for the CoMesh FPBA.

When downloaded into CoMesh, the design is not only fully functional, it is fully timed, operating at a guaranteed 300 MHz for five-levels of logic. Prior to generating the configuration file, the designer sets performance parameters for the hardware: timing specifications, hardware size and cost limits, power consumption, even processing time for the compilation. Given reasonable limits, the CoMesh chip is up and running within the hour. And running faster, smaller, and with more stability than any competitive reconfigurable products.

Continuing scenario

It's 9:20pm, the design is working in silicon, verified as correct. "Should we see how small we can get this overnight?" asks one of the engineers. As the words escape his month, the VP of marketing walks by. She always works late. "What have you got?" The engineers grin, "it's the product design we discussed this morning, running in CoMesh!" "Great," she says, "let's ship it in the morning."