LOSP SYNTHESIS SYSTEM: COMPARATIVE CAPABILITIES

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CONTENTS

VLSI circuits are perhaps the most complex artifact made by man. Their design and manufacture requires an extensive range of skills and processes. Since Electronic Design Automation (EDA) tools have evolved via accretion, EDA market leaders have dozens of products, each applying to a different aspect of the design and fabrication tasks.

The following charts summarize the current state-of-the-art for EDA products, and indicate the relative strengths of tools in the Losp synthesis system. These comparisons reflect existing prototype Losp boundary logic tools; the complete Losp suite of innovative EDA technologies is intended to cover all design categories, in a fully integrated single design tool.

Losp Functional Capabilities

The capabilities of the Losp synthesis system are indicated below for Boolean and EDA tasks. All tools are implemented, except those marked with a *tilde* (~). The marked tools have been designed into the Losp system, but have not yet been implemented.

General Boolean Capabilities

- evaluate logic expressions in given binding environment
- minimize logic expressions algebraically
- identify tautologies
- determine satisfiability and generate counterexamples
- perform partial function evaluation
- minimize variable references
- identify necessary sequential components of a design
- identify parallel components of a design
- standardize logic representations
- verify equivalence of structurally different forms
- Boolean factoring
- Boolean pattern abstraction
- case analysis
- ~ identify abstract symmetries
- ~ Boolean constraint reasoning

EDA Specific Capabilities

- parse EDIF, VHDL and Verilog circuit descriptions
- optimize combinational and sequential multilevel designs
- remove redundant logic
- detect false paths and minimize reconvergent fanout
- remove don't care conditions
- reduce delay along critical path
- reduce gate count or area
- trade-off delay and interconnect
- optimize structure sharing in multilevel circuits
- specify fanin and fanout limits
- generate designs to meet multiple objectives
- technology mapping for xor, mux, nLUT, others
- simulate functionality with bit-streams
- ~ identify abstract patterns, construct library elements
- ~ identify equivalent circuits and pin-point differences
- ~ identify patterns and hierarchical decompositions
- ~ generate test vectors

Controllable Design Parameters

- low-redundancy (literals, forms, distribution of forms)
- CNF/DNF, SOP/POS
- Implicate Normal Form (deepest nesting)
- generalized nand/nor
- four-input look-up tables
- specific gate sets: {nor, not},{and, or, not},{and, or, not, mux, xor}
- specified fanin and fanout
- structure sharing (increased fanout, decreased area)
- maximal structure sharing (disassemble and reconstruct)
- depth/interconnect tradeoffs (critical path reduction)
- low-level abstraction (xor and if-then-else/mux units)
- ~ high-level structural abstraction (specific to functionality)
- ~ specific structural partitioning (designated library modules)

Methodologies and Tasks

A leading EDA software vendor partitions its product offerings into functions (design methodologies) and behaviors (design tasks). Methodologies organize product groups, tasks organize market segments. The applicability of the implemented Losp algorithms is marked by from 0 to 3 *asterisks*. More asterisks mean more applicability.

Design Methodologies	*Losp*
• functional verification	***
• logic synthesis	***
• static verification	***
• FPGA synthesis	**
• test automation	**
• design reuse	*
• physical synthesis	
• system level design	

Design Tasks		*Losp*
• design optimization		***
• functional verification		***
• logic synthesis		***
• static timing analysis		***
• testing		***
• behavioral synthesis	***	
• design for test		***
• formal verification		***
• datapath synthesis		**
• links to layout		**
• simulation		**
• automated test pattern generation		**
• FPGA solutions		**
• library development	**	
• reliability analysis		**
• testbench automation		**
• simulation models		**
~ timing verification		**
• top-level routing		**
• power solutions		**
• DSP		*
• dynamic gate-level power analysis		*
• power management and diagnostics		*
• design planning		*
• dynamic timing analyzer		
• hardware IP characterization		
• mixed HDL simulation		
• model directory		
• hw/sw co-design and co-verification		
• IP modeling		
• nanometer IC design		
• physical verification		
• RC extraction		