LOSP SYNTHESIS SYSTEM: OVERVIEW

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LOSP SYNTHESIS SYSTEM: COMPARATIVE CAPABILITIES

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Context

This paper describes the Losp boundary logic tools that contribute to the overall Project Plan. The Losp synthesis system performs logic synthesis on netlist specifications of design functionality. The synthesis decision methods are integrated with the TSMC fabrication library specifications, uniting logic synthesis with technology mapping. The core algorithms are fully functional, however minimization of registers and an engineer's interface are not yet implemented.

Summary

Current EDA tools and techniques are antiquated for today's multi-million gate semiconductor designs. EDA companies are doing their best with the mathematical modeling tools that they have, but incremental improvement of these tools is not succeeding. What is needed is a fully integrated suite of formal design and synthesis tools that scale to networks of literally billions of transistors.

Losp incorporates completely new mathematical modeling techniques that provide solutions for today's complex designs. These techniques are formal, integrated, and powerful. A formal design specification is sufficient for Losp to generate functionally correct designs that are *correct by construction*. Designers can steer the optimization engine to meet desired performance criteria.

Over the last decade, the boundary logic algorithms have been extensively tested and benchmarked against leading EDA competition. These prototype tools already outperform commercial EDA software, yielding semiconductor designs with superior time-to-market and development cost savings.

Introduction

Due to improvements in the costs and densities of physical fabrication over the last three decades, the transistor networks that constitute semiconductor circuitry have been rapidly increasing in complexity.

Due to the absence of continuing innovation in mathematical modeling, the Electronic Design Automation (EDA) software tools used to design semiconductor networks have not kept pace, and have been facing a crisis in capabilities for several years. Tools provided by the $4 billion/year EDA software industry are not adequate for specification, design entry, verification, and testing of today's complex functional designs. EDA tools and techniques that worked well for thousands of gates do not scale to millions of gates.

The rapid evolution in the nature of design is taking place in a context for which *time-to-market* and *manufacturing costs* are paramount. There is literally no time left for careful design and no money left for tailored hardware. Designers must achieve both increased performance and faster turn-around while producing inexpensive just-in-time chips. And due to the complexity of designs, designers are completely dependent upon their automated software design tools.

Where will the next qualitative leap in EDA tool performance come from?

Boundary Logic Tools Advance the State-of-the-Art

Common wisdom suggests that the semiconductor industry completely understands logic, the foundational mathematics underlying all design and indeed all computation. However, mathematical tools and techniques change over time, refining and extending what was previously known.

The Losp synthesis system implements an entirely new approach to logic that is more efficient than conventional techniques, leading to improved scalability of algorithms *in all cases*. Losp generates designs that are error-free, verified, and testable. The boundary logic used in Losp is much simpler, yet has more capabilities, than the Boolean logic currently used today by commercial synthesis systems. The ***Technical Descriptions*** provide additional information.

Losp incorporates many ground-breaking innovations in the core engines and at the interface. New capabilities include improved tools for:

- multilevel design
- controlled optimization of designs
- generation of alternatives for design exploration
- verification of the correctness of designs
- design abstraction for control of complexity
- design customization for technology mapping
- visual interface for comprehension of large designs

Comparative Capabilities presents more information. The proposed EDA tools are a comprehensive solution, providing an integrated and complete approach to design of semiconductor circuits. ***Value Propositions*** summarizes the desirability of the Losp system capabilities. Aspects of Losp have been under development for over a decade. The logic synthesis component has been benchmarked as generating significantly better area and delay optimization than leading EDA synthesis tools. ***Empirical Results*** provides benchmarking details.

Disruptive, Facilitating, Integrated

Boundary logic provides a basis for the next breakthrough in circuit design technology.

Losp is *disruptive*, improving upon the state-of-the-art by incorporating innovative mathematical techniques and algorithms that are unlike any found in commercial products. Losp is *facilitating*, providing competitively more efficient algorithms within a foundational theory that makes design faster and easier. Losp is *integrated*, removing the incompatibilities of the currently loosely organized competitive products.

Losp uses a formal *design algebra*, based on a simple non-Boolean mathematics, to produce reduced designs that meet specified performance criteria. By optimizing both logic and interconnect at the same time, Losp efficiently produces *fully testable* fault-tolerant designs without redundant components, false paths, and reconvergent paths. Losp employs *formal verification* of every design change, leading to fewer design errors and fewer design cycles. Losp integrates synthesis with technology mapping, providing efficient designs for selected target architectures including ASICs and FPGAs.

Problem Solved

Functional verification takes up 70% of design effort. This effort is growing disproportionately as gate counts increase, making verification "a nightmare".

The Losp advantage is simple: its foundation is built on a better way of working with logic. Losp can efficiently generate functionally invariant circuits across a wide diversity of specified configurations and circuit types (ASIC, DSP, ALU, PLA, FPGA, etc). Losp modifies designs in controlled, incremental steps, providing an ability to generate circuits that meet pre-specified design criteria without time consuming design iterations. Losp permits a designer to steer the system's output through a diversity of delay and area trade-off points, selecting the performance that is most desirable for a particular design.

The Losp implementation of boundary logic is backward compatible with existing design techniques and existing circuit specifications. Learning new skills and mastering new tools is not necessary. Designers can go from functional specification to verified netlist at the push of a button, while generating designs with superior performance.

The problem with EDA software is antiquated mathematical tools. The solution is boundary logic, implemented in the Losp synthesis system.