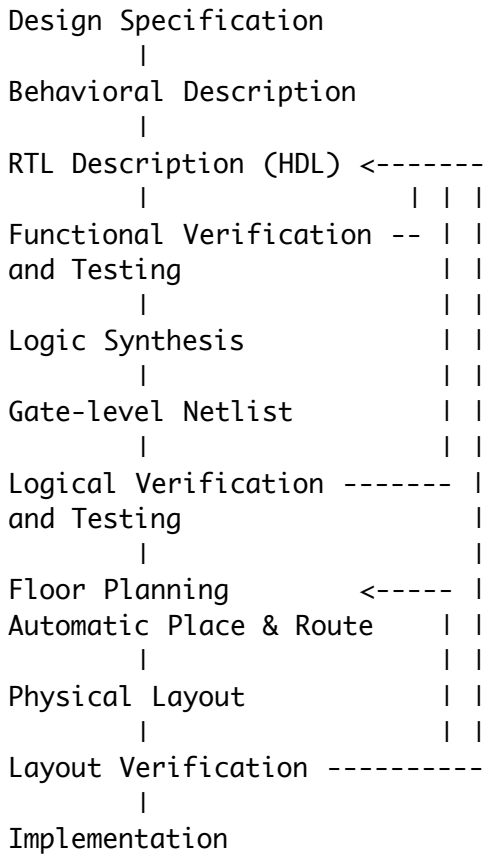
SOME DESIGN FLOWS

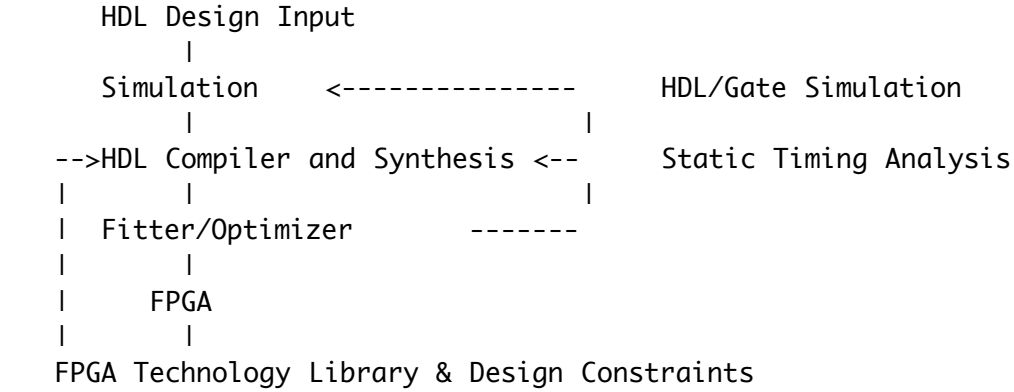
William Bricken

January 2002

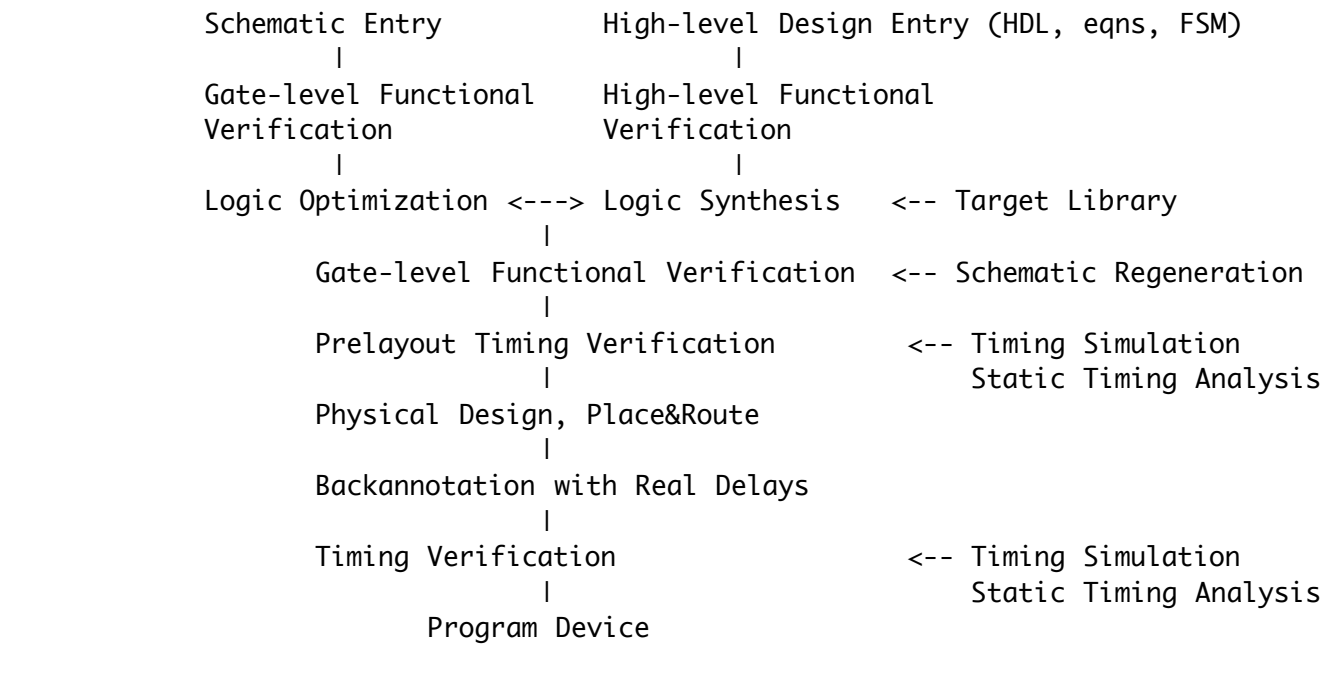
GENERIC



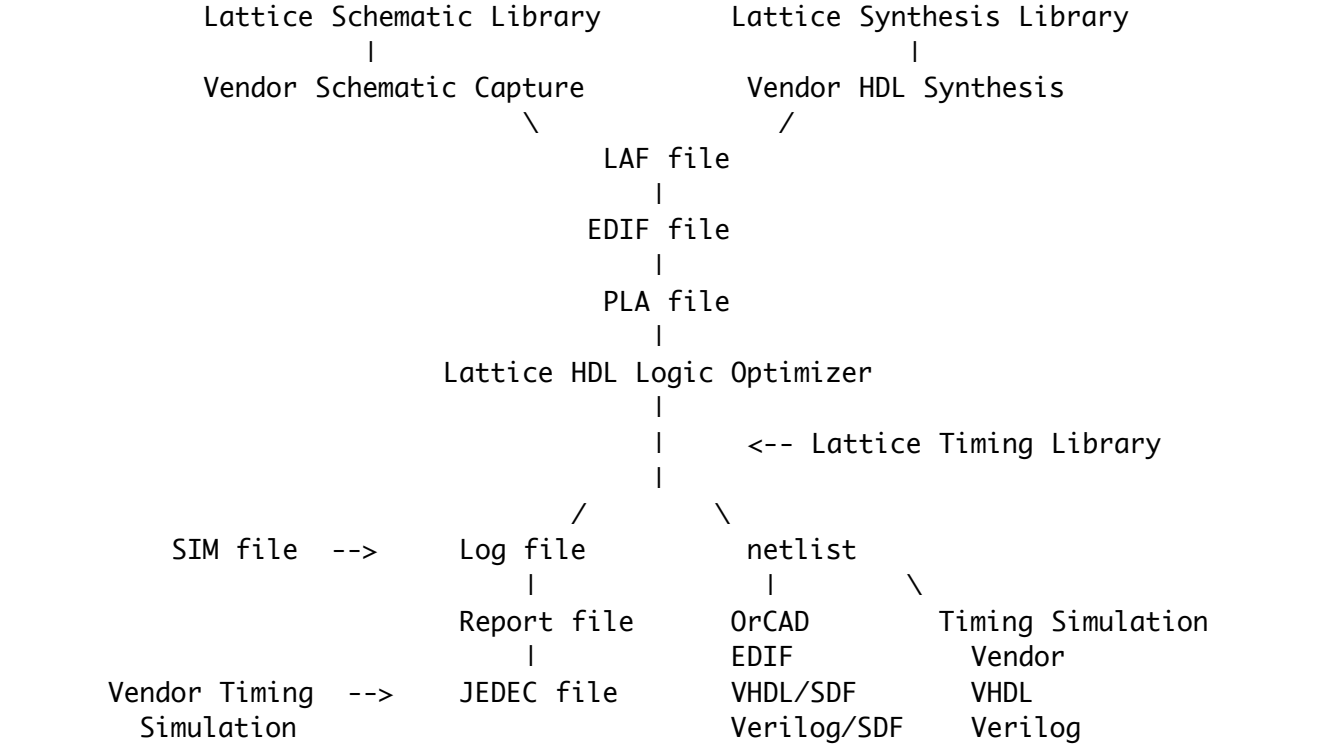
FPGA



STANDARD CONVERGENT



LATTICE



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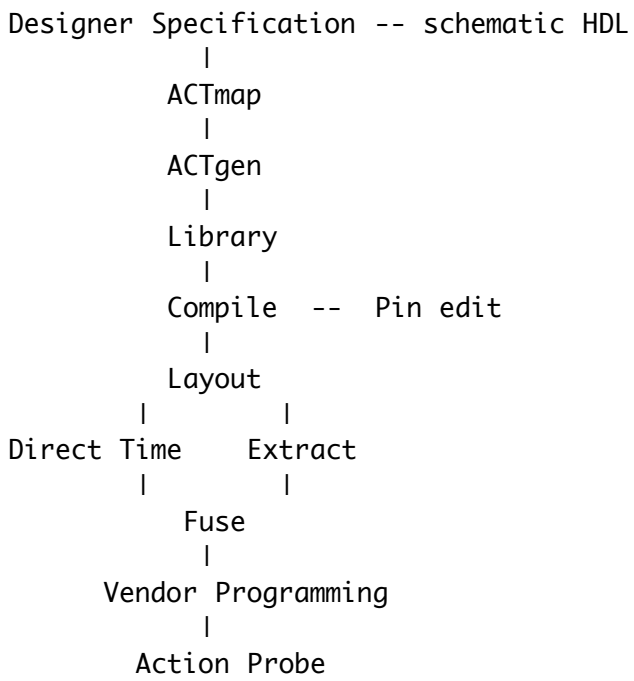
ACTEL



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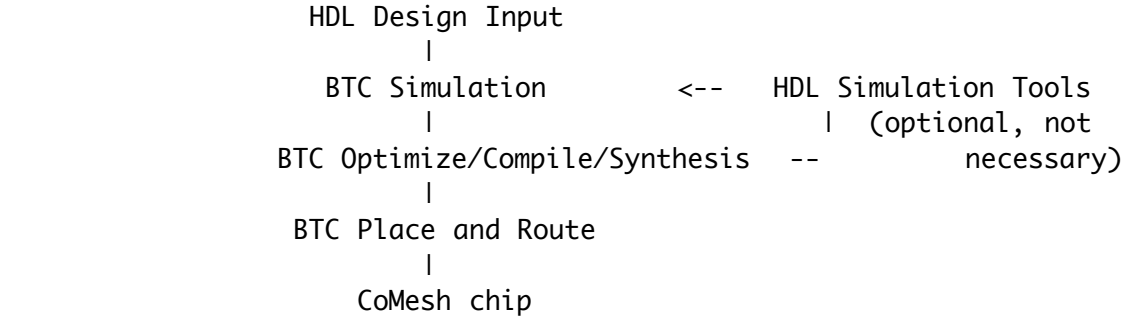
COMESH



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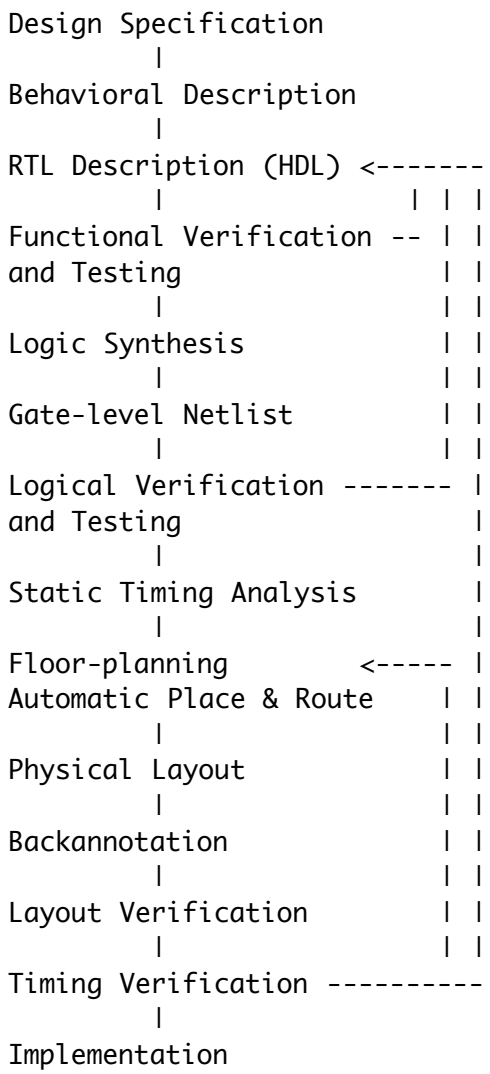
HYBRID


Design Specification
Behavioral Description
RTL Description (HDL)
Functional Verification and Testing
Logic Synthesis
Gate-level Netlist
Logical Verification and Testing
Static Timing Analysis
Floor-planning
Automatic Place & Route
Physical Layout
Backannotation
Layout Verification
Timing Verification
Implementation

COMPARE GENERIC TO COMESH