Bricken™ Technologies

Bricken Technologies Corporation

Executive Summary

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FORWARD LOOKING STATEMENTS

This document does not constitute a solicitation or offer to sell securities of the Company.

Some of the matters discussed in this document include forward-looking statements. We have based these forward-looking statements on our current expectations and projections about future events. In some cases, you can identify forward-looking statements by terminology such as “will,” “expect,” “believe,” “anticipate,” “intend,” “plan,” “estimate,” and similar expressions (or the negative of such expressions). These statements are based on our current beliefs, expectations and assumptions and are subject to a number of risks and uncertainties. Actual results, levels of activity, performance, achievements and events may vary significantly from those implied by the forward looking-statements.

TRADEMARKS

CONTACT INFORMATION

Bricken™ Technologies

COMPANY OVERVIEW

Bricken Technologies Corporation (“BTC” or “Company”), a Delaware corporation founded in March 2001, is a development stage company established to commercialize existing core technologies created by Dr. William Bricken and now owned by the Company. Based on BTC’s novel and proprietary Iconic Logic™ algorithms, these core technologies include several unique computational architectures and related families of semiconductor products.

The Company’s first products are a reconfigurable logic hardware device and related optimizing compiler software used to create the downloadable circuit configuration for that device. The patent-pending Bricken Iconic Logic™ Device (the BILD™ chip) is expected to be very competitive in $4.1 billion programmable logic device market. Within the programmable logic device market, the Company is targeting and anticipates success in acquiring market share in the $1.2 billion market for Complex Programmable Logic Devices (CPLDs) and in the $2.7 billion market for Field Programmable Gate Arrays (FPGAs).

Programmable logic devices (PLDs) are used by original equipment manufacturers in a broad range of vertical markets, including communications, computers, industrial equipment, consumer appliance, military, and automotive applications. Because of their more stringent performance requirements, our follow-on PLD markets include medical, military and space applications.

Compared with CPLDs, BILD™ chips offer far better scalability, while enhancing both design flexibility and ease of reprogramming. When compared with FPGAs, BILD™ chips offer important cost, power, and design flexibility advantages. In addition, engineers will not have to address often difficult timing, placement and routing, and resource allocation design issues. BTC also expects its products to have higher clock speeds, require significantly less power, and be up to an order of magnitude less expensive to fabricate.

BTC will operate as a fabless semiconductor company. The Company expects to sell its Bricken™-branded hardware products through traditional channels and, in some instances, directly to customers. Channels include manufacturer's representatives and distributors of electronic components.

As a major element of the Company’s vertically integrated product offering, BTC will license directly to its chip customers without cost its Iconic Logic™ Optimizing Compiler software used to program BILD™ chips. The Internet will be the principal communications channel for software distribution, documentation, and hardware and software support.

The Company has completed its first hardware simulation of a BILD™ chip running on a FPGA. A first version of the Iconic Logic™ Optimizing Compiler is fully implemented and operational.

The Company presently owns and is continuing to develop what it believes will be regarded as "pioneering" intellectual property. BTC has filed three patent applications in the United States and intends to file additional applications in both the United States and in commercially important foreign jurisdictions.

INITIAL MARKET OPPORTUNITIES

Three principal types of digital integrated circuits are in common use: microprocessors, memory and logic. Microprocessors are used for intensive control and computing tasks and require software programming to define their functionality. Memory is used to store programming instructions and data. Logic is used to manage the interchange and manipulation of data within a given system.

BTC products based on the Bricken Iconic Logic™ Device (BILD™) architecture are expected to be very competitive in segments of the programmable logic device market and later on in segments of the 8-, 16-, and 32-bit embedded microprocessor and microcontroller markets. Programmable logic devices are widely used semiconductor components that can be configured for a specific functionality by the end customer. The Company's intended initial market entry point will be a closely related family of products with exceptional competitive advantages over CPLDs and low-end FPGAs.

The market for programmable logic devices is large with substantial growth opportunities. Dataquest estimated the overall programmable logic market to be $4.1 billion in 2000.[1] Within this market, the CPLD market is estimated to be about $1.2 billion while the FPGA market is estimated to be $2.7 billion.

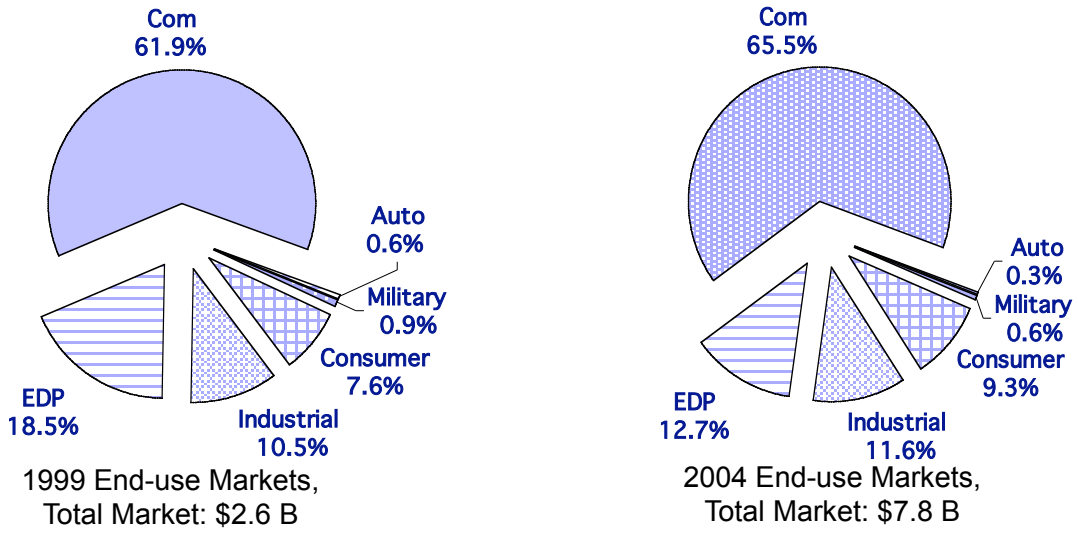

Figure 1: PLD Market Share 1999, 2004

Cahners In-Stat has similar numbers for the size of the market and additional statistics on vertical markets that are the major customers for PLD products. Figure 1 shows market size and vertical market share in 1999 and 2004. The communication application market is by far the largest vertical market for programmable logic devices. Other markets include computing, industrial, consumer products, military, and automotive applications.[2] Although these estimates were published prior to the current recession, they do suggest that as economic recovery takes hold the market for programmable logic devices should grow at a pace that far exceeds overall economic growth.

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[1] Quoted in Lattice Semiconductor's 2000 SEC 10-K, page 3. Others estimate the PLD market as growing from $2.9 billion in 1999 to $5.6 billion in 2000 (www.ebonline.com/story/OEG20010604S0103, IC Insights quoted in "PLDs/FPGAs", Electronic Buyers Network, 6/06/01). Although different sources arrive at different market estimates, they agree that the market is in excess of $2 billion with significant growth potential.

[2] "UPL [User Programmable Logic] Market Forecast: 1999-2004," Cahners In-Stat Group, 2000.

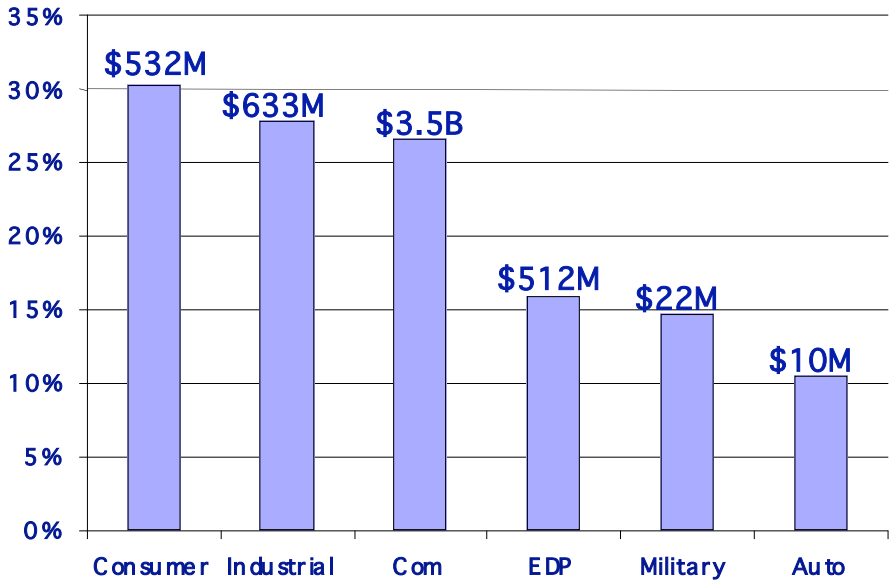

Figure 2: CAGR and Estimated Market Growth by Market Segment

In an expanding economy, the consumer appliance and industrial markets are expected to show the largest percentage compound annual growth rates (CAGR) with communication applications growth just behind (Figure 2). Although other segments are expected to show higher percentage growth rates, the communications market segment is expected to show the largest absolute growth 1999-2004, namely $3.5 billion over this 5-year period. The industrial, consumer, and computer (Electronic Data Processing, or EDP) markets are forecast to grow $500 million to $600 million over the same period. In these markets, BILD™ chips are expected to successfully compete with CPLDs and FPGAs from market leaders such as Altera, Cypress, Lattice, and Xilinx.

Challenges Addressed

The family of BILD™ architecture products will address the following technical and market challenges:

- Eliminating CPLD scalability constraints
- Greatly simplifying timing and resource allocation
- Eliminating place and route considerations
- Enhancing design ease and flexibility
- Maintaining backward compatibility with current design practices
- Requiring no new manufacturing techniques or processes
- Leveraging the economics of memory rather than of logic
- Significantly reducing time-to-market
- Substantially lowering power consumption
- Improving computational efficiency and processing speed
- Lowering chip cost and total cost of ownership

CPLDs

Complex Programmable Logic Devices are currently used to enhance product time-to-market, to reduce non-recurring engineering costs, and to increase product verifiability and reliability, without the development overhead associated with Application Specific Integrated Circuits (ASICs) or with custom integrated circuits. More specifically, CPLDs are optimal for various control logic applications, such as encoders, decoders, state machines, bus arbitration, and sequencers.

Until recently, CPLDs have been limited to relatively small functions with a modest number of logic gates. Leveraging smaller physical feature sizes, Cypress and Lattice have brought to market much larger CPLDs that claim to support larger numbers of gates. These devices are intended to support the trend toward logic integration on a single chip.

Larger capacity products notwithstanding, CPLDs do not scale well. BILD™ technology eliminates the scalability problems associated with two-level logic architectures (the basis of all current CPLDs) while delivering the advantages usually associated with CPLD architectures: lower power consumption, lower price, faster performance, sound verification, and improved ease-of-use. In addition, BILD™ chips will provide significantly improved resource allocation while eliminating problems associated with place and route and timing management. The Company expects that its high density BILD™ chips will compete very effectively with current CPLD products of any capacity and with their successor products anticipated to be in the marketplace in the next 18 to 24 months, and beyond.

FPGAs

FPGAs are used to enhance time-to-market, to eliminate the overhead of ASIC design, and to standardize products on a common reprogrammable architecture. FPGAs, however, are inefficient, both in computational speed and in fabrication die size. FPGAs are large because they provide routing resources that are never again used once the device is programmed. FPGAs are slow because this routing is complex and inefficient.

The Optimizing Compiler for the BILD™ reconfigurable architecture generates stable and predictable timing automatically, with fully utilized logic resources. The BILD™ architecture eliminates placement and routing by eliminating programmable interconnect. BILD™ chips improve upon FPGAs by providing stable and verifiable behavior. The BILD™ technology provides a faster time-to-market, with an easier-to-design, higher-performance product that is less expensive to fabricate.

An increasingly important FPGA market segment is the use of these devices for System on a Chip (SoC) applications. Xilinx's Virtex-II FPGAs provide significant resources in support of SoC applications. While their largest device claims to support a million gates, around 170K gates are actually allocated to logic while the remaining resources can be used only as memory.

Future BTC products will compete effectively in this market because the BILD™ architecture makes far more efficient use of resources. The logic portions of SoC applications are optimized and efficiently stored on the BILD™ chip. Additional resources will be efficiently devoted to memory use since much of the BILD™ chip is memory anyway. Thus we believe that future BILD™ architecture products will be extremely competitive in this market from a price/performance standpoint.

ASICs and Custom Chips

Custom and application specific chips have superior performance characteristics since they are designed and manufactured for a specific, targeted functionality. ASICs have no waste, they do not have to provide flexible interconnect, they do not have to accommodate a diversity of logic capabilities, and they can be optimized for speed, power usage, and ease of manufacturing. To achieve these advantages, ASICs have relatively huge non-recurring engineering costs (NRE), they take a long time to design, and once manufactured, they provide no flexibility to meet changing needs and inventories. For these reasons, ASICs

cannot be cost-justified unless manufactured in large quantity (>100,000 units). In today's rapidly evolving marketplace, the time-to-market delay of ASICs, which may be years, is threatening to obsolete them as competitive products.

Due to a simple and homogeneous architecture based on memory densities, BILD™ chips can achieve performance levels comparable to ASICs without their development costs or their performance rigidity. BILD™ products provide the best of both the custom and the reconfigurable worlds by combining the flexibility of dynamic reconfiguration with the efficiency of customized design. The Company expects that its products will be cost-effective replacements for ASICs in quantity 500,000 or less per design.

Microcontrollers and Embedded Microprocessors

BTC also expects its BILD™ products to acquire market share from producers of the nearly 6 billion 8-, 16-, and 32-bit microcontrollers and microprocessors manufactured annually.[3] (A microcontroller is a type of microprocessor with functionality limited to a specific control task.) While simplifying conventional design flow, the BILD™ architecture provides an improved hardware solution that will be especially attractive for real-time applications where speed combined with very low power consumption are of particular importance.

BILD™ products will also strongly appeal to those who wish to move their software-programmed microcontrollers and embedded microprocessors to dedicated hardware designs in order to take advantage of hardware speeds, lower power consumption, and verifiably correct operation. For these applications, the dedicated design is stated in a Hardware Definition Language and then directly and automatically converted into a BILD™ hardware solution.

BRICKEN ICONIC LOGIC DEVICE ARCHITECTURE

The BILD™ architecture defines an entirely new class of reconfigurable logic devices that combines the performance of multilevel ASICs with the efficiencies of CPLDs.

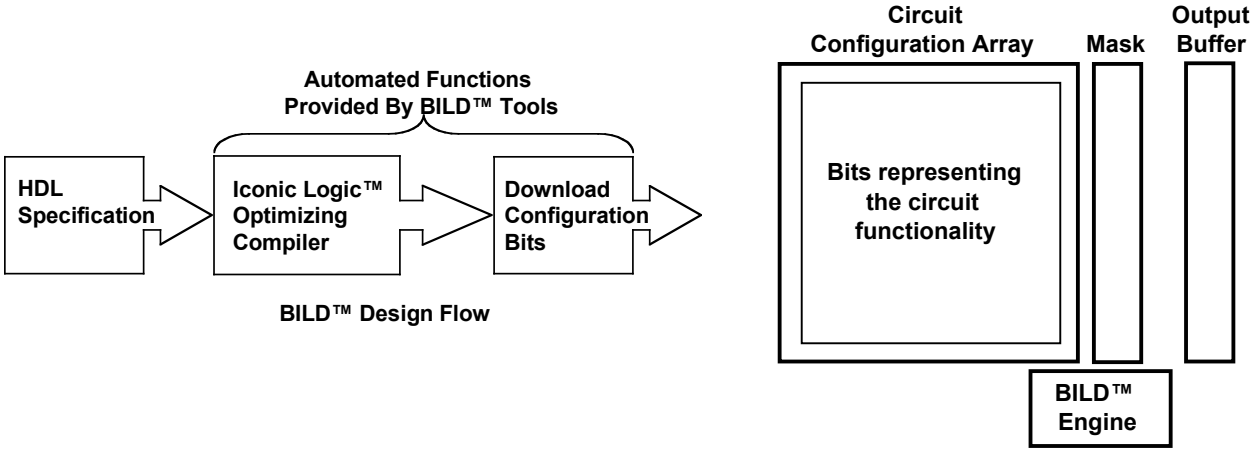

Figure 3: BILD™ Design Flow and Chip Architecture

BILD™ Chip Design Flow

To configure a BILD™ chip, an engineer first specifies the desired functionality using the synthesizable subset of an industry standard Hardware Definition Language (HDL) such as Verilog or VHDL. The Iconic

[3] David Tennenhouse, "Proactive Computing," CACM 43-5 March, 2000.

Logic™ Optimizing Compiler then generates a set of configuration bits customized for the BILD™ hardware. When downloaded, these configuration bits define the circuit structure and function to a BILD™ chip.

Circuit specifications to be run on BILD™ chips require no attention to the traditionally difficult tasks of logic placement and signal routing. This is where the highly innovative BILD™ architecture pays significant design dividends. Iconic Logic™ techniques standardize, automate and verify timing while completely eliminating interconnect and routing, thus allowing the designer to focus solely on specification of the desired functionality. The BILD™ architecture facilitates a shorter, easier design process while still providing both the efficiencies of ASICs and the cost benefits of PLDs.

BILD™ Chip Operation

The BILD™ hardware consists of four main components (Figure 3):

- the Circuit Configuration Array (CCA), which stores the static circuit configuration,
- a small register bank (Mask),
- an Output Buffer, and
- the ultra-lightweight BILD™ Engine, a silicon implementation of certain Iconic Logic™ algorithms.

Circuit configurations are evaluated in four steps:

(1) inputs are written into the Mask;

(2) the BILD™ Engine evaluates the static configuration bits within the CCA in the context of the Mask state, and writes partial results back into the Mask and into the Output Buffer;

(3) to complete the computation, the Engine again evaluates the configuration bits in the context of the new Mask state; then

(4) outputs are read from the Output Buffer.

Since only the Mask and Output Buffer change state, computation draws extremely low power. Also, since evaluation is achieved directly in hardware, computation is extremely efficient and reliable. Further, since the CCA can be rapidly and easily reconfigured, BILD™ chips have complete dynamic functional flexibility.

Internally, the Engine requires as few as four system clock cycles to evaluate a combinational function. Externally, these four clock cycles define the timing interface. For sequential circuits, the Engine functions as a pipeline with four clock cycles between register banks. This performance is predictable regardless of the conventional timing and wiring complexity of the circuit.

By expressing logic functionality as an abstract spatial pattern within the CCA, the BILD™ architecture removes significant design impediments. BILD™ chips do not use interconnect logic, do not require logic placement, and do not incorporate routing between logic blocks. Instead, the fundamentally innovative BILD™ architecture expresses logic functionality in the static array of CCA bits.

Implementation Choices

The BILD™ architecture is the foundation for a family of products for both reconfigurable and fixed-function devices. The CCA can be manufactured using a variety of memory-like bit storage techniques, providing a broad range of BILD™ product performance and cost characteristics (Figure 4). For example, the CCA array can be implemented with any of these common bit-storage techniques:

- Static RAM: very fast, relatively expensive, low density, high power, rapidly reconfigurable, volatile
- Flash ROM: very fast, inexpensive, high density, rapidly reconfigurable, non-volatile
- Hardwired ROM: fastest, least expensive, highest density, very low power, non-reconfigurable, non-volatile

Strictly speaking, the Circuit Configuration Array is not a memory since it does not require address decoding and since the rows are not accessed sequentially. Instead, the entire CCA is activated in parallel. The different bit-storage architectures simply provide different levels of performance, reconfigurability, and cost.

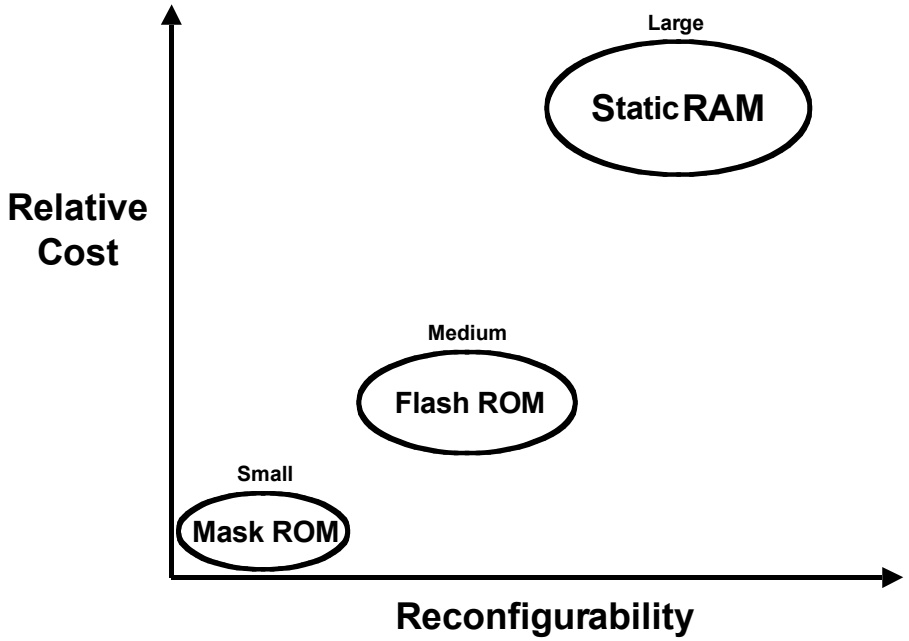

Figure 4: Example CCA Materials by Cost, Reconfigurability, and Die Size

Mask ROM CCAs achieve extremely low cost for higher volume applications at the expense of reconfigurability. Flash ROM versions of BILD™ chips provide the best balance of lower cost with just-in-time dynamic reconfigurability. When requirements include frequent reconfigurability combined with locally available memory, higher unit cost Static RAM CCAs may be preferable.

However, it should be noted that the programming for any BILD™ chip is the same regardless of the type of CCA bit storage architecture. As the functional specifications of a semiconductor product mature, companies will be able to migrate from higher cost, easily reconfigurable BILD™ chips to much lower cost, lowest power consumption, highest density hardwired ROM BILD™ chips appropriate for higher volume applications.

The price/performance of memory technologies is improving faster than other hardware technologies. Accordingly, the competitive advantage of BILD™ architectures should outpace all other silicon computation techniques.

COMPARATIVE PERFORMANCE

The variety of hardware and microprocessor architectures in products today addresses a diversity of requirements. Cost is paramount; however, many applications emphasize other factors, such as time-to-market, ease of modification, computational performance, and verifiable correctness. The table below compares the relative benefits of several common architectures. Entries have been standardized so that a ++ rating is highly desirable, a -- rating is highly undesirable.

FEATURE	BILD	CPLD	FPGA	ASIC	Custom Chip
Time-to-market	++	++	+	-	--
Ease of design	++	+	--	-	-
Ease of place and route	++	-	--	+	+
Ease of timing management	+	-	--	+	++
Ease of resource allocation	++	+	-	-	--
Ease of verification	++	+	--	-	-
Speed	+	+	-	+	++
Density	+	-	--	++	++
Low power use	+	-	--	++	++
Program I/O	++	+	+	--	--
Low cost to change	++	+	++	--	--
Scalability	++	-	+	++	++
Low manufacturing cost	+	-	--	+	+
Low non-recurring engineering costs	+	+	+	--	--

As the comparison chart indicates, the BILD™ architecture addresses and solves several problems associated with other common architectures. BILD™ hardware products combine the performance qualities of simple custom hardware with the benefits of FPGA homogeneity and reconfigurability. Additionally, BILD™ products provide formal verification, automated design, predictable performance, and very low cost. The result is a completely new approach to time-to-market: fast and easy design with minimal overhead and risk.

Better Than CPLDs

Considering performance, manufacturing cost, power usage, design overhead and risk, verifiability, field reliability, and time-to-market, a simple two-level PLD (SPLD) architecture is best, offering ASIC performance without the accompanying design and manufacturing costs. However, SPLDs have two significant flaws. First, since SPLDs use two-level logic, they do not scale to larger functions. Second, SPLDs provide a fixed logic resource that limits design choices. CPLDs have addressed scalability to some extent; however, their compromise results in a hybrid architecture with some of the limitations of SPLDs and some of the limitations of FPGAs. The BILD™ architecture provides all of the benefits of both SPLD and CPLD approaches, while maintaining scalability by enabling the use of multilevel logic. These benefits include:

- Verifiability through known formal methods.
- Predictable timing and capacity.
- Low manufacturing cost.
- Very low power requirements.
- Homogeneous architecture which is very easily reconfigured.

Better Than FPGAs

FPGAs pay for the cost of reconfigurability with on-chip routing and testing which is not completely used when the chip is deployed. Compared with FPGAs, BILD™ chips have these advantages:

- No place and route, resulting in more efficient use of area and in easier design. These translate directly to lower costs and faster time-to-market.
- No timing variation due to place and route choices. This makes design far easier while lowering time-to-market risks such as unpredictable timing and capacities.
- Complete freedom of I/O pin placement. FPGA designs require locked pin locations, making board-level integration difficult.
- Dynamic reconfigurability. Reconfiguring a BILD™ chip is as easy as loading memory.

Another route to reconfigurability is to use a microprocessor. The cost here is around two orders of magnitude slower performance. For this reason, modern FPGA architectures outperform custom DSPs. Due to limited interconnect, FPGAs are not well suited for complex control tasks; instead, they excel at register intensive tasks such as computer arithmetic. BILD™ chips handle all types of computational tasks, including complex control with real-time constraints, without compromising performance.

Better Than ASICs

Like CPLDs and FPGAs, BILD™ chips are dynamically reconfigurable, providing significant advantages over ASICs:

- Faster time-to-market.
- Low design risk, low NRE design.
- Ease of reconfiguring to new protocols and functions.
- Volume production not necessary, low inventory risk.
- Software download in place of masking, test vectors, wafer fabrication, and packaging.

The benefits of ASICs are limited to better performance and to less expensive manufacturing for high volumes. Unlike other reprogrammables, BILD™ chips are competitive with ASIC technology in both cost and performance. The BILD™ Engine is expected to operate in the GHz clock range. The BILD™ CCA is expected to reach ASIC densities (4000-8000 gates/mm^2).

Competitor Product Comparisons

Using publicly available product information, we compared BILD™ architecture products with popular products from Xilinx and Altera.

The Xilinx XC4010XL FPGA is a standard mid-range product. It has .35um feature size, a 72 mm^2 die size, claims to support up to 20K gates (10K gates is acknowledged to be more realistic), and retails for $62. A competitive BILD™-FlashROM chip of 72 mm^2 supports 75K gates for the same retail price. Alternatively, a comparable 20K gate BILD™ chip could sell for $16 and is expected to cost less than 60 cents to fabricate.

The Altera EPM7256A EEPROM is a high-end reprogrammable SPLD. It has a 40 mm^2 die size and accommodates 5K gates (a realistic number, given that some functions cannot be expressed). In contrast, a competitive BILD™-FlashROM chip of 40 mm^2 would support over 50K gates, has no limits on expressability, no fixed resource constraints, no register limitations, and no scaling problems. Alternatively, a BILD™-FlashROM chip supporting 5K gates would require about 1.25 mm^2 and is expected to cost less than 12cents to fabricate.

The Xilinx XPLA3-128 CoolRunner CPLD is a mid-range, low-power product with a capacity of about 5K gates (as estimated by the number of macrocells needed to express several common circuit functionalities). Die size data for this product is not publicly available. A competitive 5K gate BILD™ chip would require only 1 mm^2 of chip area and use far less power. The fabrication cost for 1 mm^2 of a BILD™ chip is expected to be less than 10 cents.

ICONIC LOGIC™ OPTIMIZING COMPILER

Used to program BILD™ chips, the Company's Iconic Logic™ Optimizing Compiler takes as input an industry standard HDL description of the circuit functionality. The untimed synthesizable subset of Verilog is sufficient, but any HDL will do. Compilation is straightforward: the Iconic Logic™ Optimizing Compiler takes minutes to complete the compilation process and then writes a file containing the configuration bits used in conjunction with a BILD™ chip.

Time-to-market is of primary importance since it determines the shelf life of a VLSI product. This is where the Company's Iconic Logic™ Optimizing Compiler excels:

- Iconic Logic™ configuration software is completely formal, assuring that a design does not stray from its golden standard.
- Iconic Logic™ software is fully automated, allowing a designer to go from HDL specification to chip configuration in hours.
- Due to its homogeneous architecture, Iconic Logic™ configuration and resource management is highly predictable.

PRODUCT STATUS

A complete first version of the BILD™ reconfigurable chip including the BILD™ Engine is operational as a hardware simulation running on a FPGA. A first version of the Iconic Logic™ Optimizing Compiler is fully implemented and operational.

The BILD™ chip is an essential component of BTC's initial product offerings. The Company's product pipeline includes second generation Iconic Logic™ architectures that require fewer clock cycles for each circuit evaluation. These next generation designs are currently implemented as software simulations. The Company is actively developing additional hardware applications of its proprietary Iconic Logic™ technology.

BUSINESS MODEL

BTC will operate as a fabless semiconductor company. The Company expects to sell its Bricken™-branded hardware products through traditional channels and, in some instances, directly to customers. Channels include manufacturer's representatives and distributors of electronic components.

To encourage adoption of the Company's hardware products, BTC intends to license its Optimizing Compiler for use with its BILD™ chip products without cost. Software, documentation, and support will be offered over the Internet.

In addition to product revenue, BTC may also license its Intellectual Properties for specific market applications where market size or market structure indicate that licensing is the preferred strategy.

INTELLECTUAL PROPERTY CREATION AND PROTECTION

The Company presently owns and is continuing to develop what it believes will be regarded as "pioneering" intellectual property. BTC has filed three patent applications in the United States and intends to file additional applications in both the United States and in commercially important foreign jurisdictions. The Company is also plans to file trademark applications in the United States and in other commercially significant jurisdictions. Where appropriate, the company will apply for copyright registration for selected materials.

FINANCING, USE OF PROCEEDS, AND STATUS

The Company is seeking a total of $10 million in a Series A preferred equity financing. Of the $10 million, $1 million is seed capital in the form of a Convertible Note financing that includes warrants.

BTC intends to use the proceeds of this financing to:

(i) build engineering, marketing, sales, and management teams;

(ii) accelerate development of BTC's hardware products and produce product samples;

(iii) acquire hardware and software to develop semiconductor products;

(iv) protect the Company's Intellectual Property;

(v) develop and implement marketing and sales programs; and

(vi) build Company infrastructure including support staff.

To date the Company has raised $350,000. Upon completion of raising the seed round ($650,000), BTC will hire the key engineering personnel and acquire the necessary hardware and software to commence development of the Company's hardware products. Additionally these funds will be utilized to further obtain and analyze market data with respect to finalizing the Company's market entry strategy.

The balance of the Series A preferred round ($9 million) is forecasted to take BTC through the production of customer product samples within approximately 15 months and to the acquisition of the Company's first customers.

MANAGEMENT – OFFICERS AND DIRECTORS

William Bricken, Ph.D.—Vice Chairman, Chief Scientist, Director and Founder

Dr. Bricken has spent over 20 years developing the tools and techniques of iconic mathematics. He has published widely in the fields of artificial intelligence, virtual reality, and education. Dr. Bricken was an Assistant Professor of Computer Science and Software Engineering at Seattle University, Seattle, Washington, from 1996 to 2001; Research Associate Professor of Education at the University of Washington from 1992 to 1995; the Principal Scientist of the Human Interface Technology Lab at the University of Washington, specializing in virtual reality design, software, and hardware technologies, from 1990 to 1994; Lecturer in Education at the University of Hawaii at Hilo from 1976 to 1979; Assistant Professor of Social Psychology and Education at the State College of Victoria, Rusden, Melbourne, Australia, from 1973 to 1975; and Principal and Founder of Coonara Primary School, Melbourne, Australia, from 1972 to 1975.

In industry, Dr. Bricken was a consultant to Interval Research Corporation, Palo Alto, California, from 1993 to 2000; CTO of Virtual Express, a virtual reality start-up, in 1994; the first Distinguished Fellow, and Director of the Research Lab at the computer-aided design industry leader Autodesk, in Sausalito, California during 1988 and 1989; Principal Research Scientist at Advanced Decision Systems, which contracted to the US Department of Defense for artificial intelligence research, from 1984 to 1988; and a Wizard at Atari Research Lab, Sunnyvale, California, exploring advanced concepts for gaming, during 1983 and 1984. University of California at Los Angeles, B.A., Social Psychology, 1967; Monash Teachers College, Melbourne, Australia, Diploma of Education, 1972; Stanford University, Stanford, California, M.S., Statistics, 1984; Stanford University, Ph.D., Mathematical Methods of Research, School of Education, 1987.

COMPANY'S ADVISORY BOARD AND CONSULTANTS