FEATURES AND SIZES

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Relative Areas

Let the feature size be "s". Relative sizes of components, parameterized by feature size:

1 bit FlashROM	= .05	= .05	s^2
1 bit DRAM	= .1	= .1K	s^2
1 bit SRAM	= 1	= 1.2K	s^2
1 flip-flop	= 4	= 5 K	s^2
1 ASIC gate	= 4	= 5 K	s^2
1 4-LUT	= 400	= 500 K	s^2
	= 30	= 40 K	s^2 PER GATE, 12 gates per 4LUT
1 CLB (XC4000)	= 1000	= 1250 K	s^2
	= 20	= 25 K	s^2 PER GATE, 50 gates per CLB
1 interconnect switch	= 2	= 2.5K	s^2
1 register file	= 1	= 1 K	s^2 per bit plus .5K s^2 per port

Relative Area and Efficiency

area

memory	= .3	(50x denser than FPGA)
custom	= 1	
MPGA	= 3	
FPGA	= 15	

area-time (processing efficiency)

custom	= 1	
mpga	= 5	
FPGA	= 100	(100-300 gate evals per sec per s^2)
uP	= 1000	(15-20 gate evals per sec per s^2)

FPGA Area

active logic	1	(generous, closer to .5)
config memory	4	
interconnect	35	

FPGA Power Use

interconnect	65%
clock	21
i/o	9
CLB	5

Densities in s^2

Type	*Range*	*Mean*
FLASH	7-26	12
ASIC	300-3000	700
FPGA	7000-57000	30000
EEPROM	50000-64000	50000

IC Industry Improvements 1981-1996

Design	20%	3K gates/person/month
Transistors	75	
Gates	100	
Memory	250	

Feature-size Ms^2/mm^2

.5	4
.35	8
.25	16
.18	31
.15	44
.13	59
.10	100
.07	204
.05	400

Type	*Cell-area s^2*	*Ratio DRAM=1*
DRAM	10-15	1
SRAM	50-100	5
EEPROM	40-60	4
FLASH	7-10	1
EPROM	9	.9
ROM	7	.7