DEMYSTIFYING ACRONYMS

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The intended uses and the peripheral support systems of an FPGA are often referred to by an assembly of rather cryptic acronyms. Each vendor provides their own unique acronyms; new technologies and refinements add new acronyms; and in general the engineering priesthood protects its own knowledge and value by making things difficult to follow.

These peripheral subsystems are all essentially simple, there are just many of them. Aside of the logic and interconnect, the capability to handle various protocols is essential. With the right hardware design, we can store various protocols, and thus be able to customize protocol capabilities to particular customers, creating a "buy what you use" model.

This list is not intended to be pedagogical or complete, and it is not well-organized. It grew out of my need to keep some of this comprehendable. Many of these acronyms show up uniquely for Xilinx products.

SUB-SYSTEMS
INTERNAL INTERFACE
- Chip-to-Chip
  - *Differential Signaling Standards*
  - *Power Protocols*
  - *Clocking*
  - *Chip-to-Memory Communication*
  - *Parallel Interface Protocols*
  - *Serial Interface Protocols*
  - *Data Transfer Modes*
- Chip-to-Backbone
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PERIPHERAL INTERFACE
- PC Display Formats
  - *Standards*
- Streaming Media Formats
- Encryption Standards

LAN/WAN/MAN COMMUNICATIONS PROTOCOLS
- Layered Model
- Internet Protocols
  - *Layers*
- Broadband/Internet Access
- Communications Protocols
- Wire Protocols
- Wireless Protocols
- Signal Encoding Protocols

PACKAGING
TESTING PROTOCOLS

SUB-SYSTEMS

These components are common; the interface to each is a small (<5000 gates, often <500 gates) specific logic configuration, usually involving buffers, encoders, decoders, comparators, converters, multiplexers, and the like.

FPGA "Field Programmable Gate Array". The field is not-at-the-factory.

ASSP "Application Specific Standard Products"

CPU "Central Processing Unit", usually a microprocessor

SDRAM "Synchronous Dynamic Random Access Memory"

LCD controller "Liquid Crystal Display"

USB "Universal Serial Bus"

PCI "Peripheral Component Interface"

EISA 32-bit bus "Extended Industry Standard Architecture"

PCMCIA slot "Personal Computer Memory Card International Association"
also "People Can't Memorize Computer Industry Acronyms"

NIC "Network Interface Card"

UART "Universal Asynchronous Receiver Transmitter"

Modem "modulate demodulate" v.34, v.90, v.any protocols

CMTS "Cable Modem Termination System"

INTERNAL INTERFACE

Communication between chips on a board, between boards in a complex system, and between computational devices over distances.

Chip-to-Chip

Differential Signaling Standards

LVDS "Low Voltage Differential Signaling" i/o protocol, switched and distributed point-to-point in parallel, uni-directional

LVPECL "Low Voltage Positive Emitter Coupled Logic" for clock transmission, 100 MHz+ interface

BLVDS "Bus LDVS" bidirectional

LDT "Large Dataset Transport" AMD specific interconnect

LVDSEXT LVDS "EXT" appears to be Xilinx only

Power Protocols

LVTTL "Low Voltage TTL" i/o power protocol, single-ended
TTL "Transistor-Transistor Logic"

LVCMOS "Low Voltage CMOS" i/o power protocol
LVCMOS33, 25, 18, 15 for 3.3V, 2.5V, 1.8V, 1.5V
CMOS "Complementary Metal-Oxide Semiconductor"

CEBus "Consumer Electronics BUS" standard powerline net

Clocking

PLL "Phase Locked Loop"

DLL "Delay Locked Loop"

Chip-to-Memory Communication

HSTL-I -II -III -IV "High Speed Transceiver Logic"

SSTL-I -II "Stub Series Terminated Logic"
SSTL2-I -II for 2.5V
SSTL3-I -II for 3.3V

Flexbus 4 12.8 Gbps 64b HSTL bus at 200 MHz

CSIX reference "Common Switch Interface Specification" 64 Gbps 32b HSTL at 200 MHz

CTT "Center Tap Terminated"

Parallel Interface Protocols

Ethernet GE = gigabit ethernets

10/100 Ethernet, 1GE, 10GE ethernet varieties

MII "Media Independent Interface" single 100Base-ethernet interface

GMII "Gigabit Media Independent Interface"

PCI 32/33 slower and older 32 MHz

PCI 64/66 528 Mbps 64b PCI, newer 64 MHz

PCI X66/100 800 Mbps 64b, 133 MHz

RapidIO 8 Gbps 8b LVDS 250 MHz

HyperTransport 3.2 Gbps 8b LVDS at 200 MHz

Serial Interface Protocols

SERDES "SERializer DESerializer"

1GE PHY 1 Gbps ethernet

XGMII reference 10 Gbps 32b XGMII HSTL bus at 312.5 MHz

AUI "ethernet Unit Interface"

XAUI any variety of AUI

SONET "Synchronous Optical NETwork"

POS PHY L3 "Packet Over SONET PHYsical Level 3" 2.48 Mbps, 32b bus at 104 MHz

POS PHY L4 "Packet Over SONET PHYsical Level 4" 11.2 Gbps 16b LVDS bus at 350 MHz

3GIO "3rd generation IO"

Data Transfer Modes

POS "Packet Over SONET"

ATM "Asynchronous Transfer Mode" family of specs 155 MBps, 622 Mbps, higher

DDM "Direct-Data Mapped mode"

DDR "Double Data Rate"

Chip-to-Backbone

5V PCI-33, 3.3V PCI-33, 3.3V PCI-X, BLVDS

GTL "Gunning Transceiver Logic terminated"

GTL+, GTLP "Gunning Transceiver Logic Plus"

AGP, AGP-2X "Advanced Graphics Port"

Board-to-Board

PCI 32/33, PCI 64/66, PCI X, POS PHY L3, POS PHY L4, Flexbus 4, and the gigabit varieties below.

PCI, RapidIO, CSIX, HyperTransport parallel

3GIO, Serial ATA, Infiniband, Gb Fiber Channel, 10GE XGMIII, 10GE XAUI, Serial RapidIO serial

PERIPHERAL INTERFACE

PC Display Formats

NTSC "Never Twice the Same Color" analog TV standard

PAL "Phase Alteration Line" 50 Hz video format (world except US)

RGB "Red Green Blue"

SECAM "Sequential Color with Memory" French "avec Memoire"

SDTV 480i, SDTV 480p "Standard Definition TeleVision"

HDTV 720p, HDTV 1080i "High Definition TeleVision"

CIF "Common Interchange Format" video encoding

AVT "Audio Video Transport"

Standards

DVB (European) "Digital Video Broadcasting"

COFDM (European) "Coded Orthogonal Frequency Division Multiplexing"

ATSC (US) "Advanced Television Systems Committee"

VSB (US) "Vestigial Side Band"

Streaming Media Formats

MPEG-1, MPEG-2, MPEG-4 "Moving Pictures Experts Group"

JPEG, MJPEG "Joint Picture Experts Group"

Real Networks format from Real Networks

QuickTime video file format from Apple

ASD "Advanced Streaming Descriptor"

Encryption Standards

DES "Data Encryption Standard"

3DES "Triple Data Encryption Standard"

AES "Advanced Encryption Standard"

PKI "Public Key Infrastructure"

CHAP "Challenge Handshake Authentication Protocol"

CMVP "Cryptographic Module Validation Program"

LAN/WAN/MAN COMMUNICATIONS PROTOCOLS

LAN "Local Area Network"

WAN "Wide Area Network"

MAN "Metropolitan Area Network"

WLAN "Wireless Local Area Network"

SNAP "Sub Net Access Protocol"

Layered Model

ISO "International Standards Organization"

OSI "Open Systems Interconnection" 7 layer protocol model

PHY "PHYsical layer" electrical, mechanical, procedural specs transmission
MAC "Media Access Control" access control for physical layer, error control and synchronization
LLC "Logical Link Control" frames source and destination addresses
UDP "User Datagram Protocol" transport
UDP socket
CODEC "COder-DECoder"

PHY varieties include
- IR "InfraRed"
- RF "Radio Frequency"
- SS "Spread Spectrum"
  - FHSS "Frequency Hopping Spread Spectrum"
  - DSSS "Direct Sequence Spread Spectrum"

DLL "Data Link Layer" LLC and MAC combined

ARP "Address Resolution Protocol" for MAC

CMSA "Carrier Sense Multiple Access" for MAC

CSMA/CD "Carrier Sense Multiple Access/Collision Detection" LAN access method

TDMA "Time Division Multiple Access" for MAC

WCDMA "Wideband Code Division Multiple Access"

RTP "Real-time Transport Protocol" for UDP

ATAPI "AT Attachment Packet Interface"

NESL "Netware Event Service Layer"

CMIP "Common Management Interface and Protocol" ISO, for network management

FAC "Forward Error Correction"

Internet Protocols

TCP/IP "Transmission Control Protocol/Internet Protocol"

TELNET "Terminal Emulation Protocol"

URL "Uniform Resource Locator"

DNS "Domain Name System"

VoIP "Voice-over Internet Protocol"

Layers

Application:	SMTP	"Simple Mail Transfer Protocol"
	POP3	"Post Office Protocol 3" (not the US Govt)
	HTTP	"HyperText Transfer Protocol"
	FTP	"File Transfer Protocol"
Transport:	UDP	"User Datagram Protocol"
	TCP	"Transmission Control Protocol"
Internet:	ICMP	"Internet Control Message Protocol"
	IMAP	"Internet Message Access Protocol"
	on top of IP "Internet Protocol"	
Network access:	PPP	"Point-to-Point Protocol"
	POP	"Point of Presence"
	SLIP	"Serial Line Internet Protocol"
	Ethernet	
Physical:	Modem, UART, Ethernet	

Broadband/Internet Access

ISP "Internet Service Provider"

ISDN "Integrated Services Digital Network"

DSL "Digital Subscriber Line"

ADSL "Asynchronous Digital Subscriber Line"

DBS "Direct Broadcast Satellite"

OIF SPI-4 "Optical Internetworking Forum Packet Interface 4"

MGT "Master Guide Table" switched and distributed point-to-point in serial

Cable

Communications Protocols

Ethernet varieties

FDDI "Fiber Distributed Data Interface" for high-speed fiber-optics

SNA "System Network Architecture" for large systems

X.25 international standard for packet-switching, WAN protocol

Wire Protocols

Ethernet

Optic Fiber

IEEE 1284 Parallel Port

IEEE 1394/Firewire fast interface standard
HAVi "Home Audio Video interoperability"

USB 1.1/2.0 "Universal Serial Bus" PC standard

IEEE 1355 lightweight serial protocol family

RS-232 serial communications port

HomePNA "HOME Phoneline Networking Alliance"

HomePlug a powerline alliance for digital connectivity

Wireless Protocols

Bluetooth 2.4 GHz band at 720 Kbps over 30 feet, very low power and cost
uses L2CAP "Logical Link Control and Adaptation Protocol"

HomeRF 2.4 GHz at 1.6 Mbps over 160 feet, medium power and cost

IEEE 802.11b 2.4 GHz at 11 Mbps over 500 feet, medium power and cost

IEEE 802.11a 5 GHz at 150 Mbps over 500 feet, medium-high power and cost

HiperLAN 2.4 GHz at 23 Mbps over 500 feet, medium power and cost

HiperLAN2 5 GHz at 50 Mbps over 500 feet, medium-high power and cost

DECT "Digital Enhanced Cordless Telecommunications"

Infrared

Signal Encoding Protocols

ADPCM "Adaptive Differential Pulse Code Modulation"

BPSK "BiPhase Shift Keying"

COFDM "Coded Orthogonal Frequency Division Multiplexing"

CWDM "Course Wave Division Multiplexing"

DFPQ "Distributed Fair Priority Queueing"

DWDM "Dense Wave Division Multiplexing"

FDQAM "Frequency Diverse Quadrature Amplitude Modulation"

PCM "Pulse Code Modulation" audio

QAM "Quadrature Amplitude Modulation"

OFDM "Orthogonal Frequency Division Multiplexing"

QPSK "Quadrature Phase Shift Keying"

TDM "Time Division Multiplexing"

VOFDM "Vector OFDM" radio

PACKAGING

SOIC "Small Outline IC"

DIP "Dual In Line"

PGA "Pin Grid Array"

BGA "Ball-Grid Array"

FPBGA "Fine Pitch Ball-Grid Array"

PQFP "Plastic Quad Flat Pack"

MQFP "Metric Quad Flat Pack"

TQFP "Thin Quad Flat Pack"

CQFP "Ceramic Quad Flat Pack"

VQFP "Plastic Very Thin Quad Flat Pack"

PLCC "Plastic Leaded Chip Carrier"

CLCC "Ceramic Leaded Chip Carrier"

TESTING PROTOCOLS

BIST "Built-In Self Test"

POST "Power On Self Test"

JTAG "Joint Task Action Group" an interface standard consisting of four pins for connecting devices in series (in a chain). Ports are TDI = test data in, TDO = test data out, TMS = test mode select, TCK = test clock. Part of IEEE 1149.1 boundary scan architecture. Can be used for loading configuration files and for testing core behavior. Consists of less than 100 logic gates.

IEEE 1149.1 Boundary Scan also IEEE 1532 a technique of surrounding the functional core of a chip with registers. The registers can be used to monitor the internal correctness of the logic core. Roughly six registers and six muxes for each i/o port.

ISP "in-system programming" Means the FPGA can be programmed without removing it from its circuit board (in system refers to the chip's external system environment). For testing, a software test package which exercises the internal logic is loaded via a JTAG interface. I/O is monitored to assure that the internal core behavior produces output which is expected from the testing input.

ICR, ISR "in-circuit reconfigurability", "in-system reconfigurability" Similar to ISP.

JEDEC "Joint Electron Device Engineering Council" protocol for identifying fuses to be set in PROM devices