# AN EXTENDED EXAMPLE OF LOSP CIRCUIT SYNTHESIS

William Bricken
October 1997

To demonstrate the capabilities of the Losp logic synthesis engine, a single circuit from the MCNC benchmarks was selected and transformed algorithmically to meet specific design objectives.

The circuit, CM85A, was selected primarily for its size: small enough to display on one page. Its structure, hidden in EDIF netlist form, was discovered during the transformation process.

The simple metrics used were

1. Nodes: a count of nodes, or gates, indicating circuit area
2. Delay: the length of the longest path through the circuit
3. Refs: the count of variable references, or wires, both internal and external, between gates, and
4. AxT: a compound measure, the product of the area, or node-count, by the time, or delay-count.

The transformation strategy was

1. remove inverters and collect XOR gates
2. distribute multiple references inward to remove redundancies
3. identify larger patterns which could be abstracted and made into library elements
4. explore various other specifications, such as FPGA mapping and fault-tolerance.

In comparison with recent (1996) published results for this circuit, our techniques performed well.

Tsai (mentor graphics) and Marek-Sadowska (UCSB),
Multilevel Logic Synthesis for Arithmetic Functions, DAC'96 p242

literals as 2input AND/OR gates:

| | | | |
|---|---|---|---|
| SIS: | 80 | CPU: | 1.7 sec in C on Sparc 5 |
| DAC: | 84 | | 1.48 sec |
| losp: | | | 0.52 sec in LISP on Mac PowerPC 8100 |

technology mapped:

| | | | |
|---|---|---|---|
| SIS gates: | 33 | lits: | 77 |
| DAC: | 41 | | 84 |
| losp: | 23 | | 47 |

The transformations and their accompanying statistics follow.

```
0.  Edif netlist for CM85A

1.  Edif-to-pun
      nodes:  76
      depth:  13
      refs:  120
      AxT:   988

2. Collapse and remove inverters
      nodes:  55
      depth:   9
      refs:   99
      AxT:   495

3.  Identify XOR nodes, assertions of variable equality and inequality
      nodes:  44
      depth:   9
      refs:   80
      AxT:   396

4.  Distribute in, removing multiple reference branches
      nodes:  36
      depth:   7     best depth = 7
      refs:   68
      AxT:   252     best AxT = 252

5.  Abstract circuit patterns, pass 1
      nodes:  32     best nodes = 32     -9 for gates
      depth:   8
      refs:   56     best refs  = 56     -9 for lit refs
      AxT:   256
      4-luts: 15     for FPGA mapping

6.

7.  Uniform NOR-gates with deep nesting and fault-tolerance
         (most fault tolerant, best lut map)
      nodes:  34
      depth:  10
      refs:   64
      AxT:   340

8.  4-LUT mapping of uniform model in 7.
      4-luts:  11    best
```

**Attachment I:** Pun-parens algebraic forms

***Form 1:*** Direct edif to pun translation

```
((cm85a)                                                    ;name
 ((a unk)(b unk)(c unk)(d unk)(e unk)(f unk)
  (g unk)(h unk)(i unk)(j unk)(k unk))                      ;inputs
 ((oa 75)(ob 73)(oc 72))                                   ;outputs
 ((   0  (43) )                                            ;gates
  (   1  (37) )
  (   2  (34) )
  (   3  (47) )
  (   4  (36) )
  (   5  (35) )
  (   6  (c) )
  (   7  (70) )
  (   8  (a) )
  (   9  (66) )
  (  10  (e) )
  (  11  (d) )
  (  12  (b) )
  (  13  (62) )
  (  14  (f) )
  (  15  (g) )
  (  16  (56) )
  (  17  (69) )
  (  18  (58) )
  (  19  (65) )
  (  20  (59) )
  (  21  (57) )
  (  22  (52) )
  (  23  (48) )
  (  24  (50) )
  (  25  (44) )
  (  26  (i) )
  (  27  (h) )
  (  28  (53) )
  (  29  (40) )
  (  30  (j) )
  (  31  (k) )
  (  32  ((31) (j)) )
  (  33  ((k) (30)) )
  (  34  ((32 33)) )
  (  35  ((29 28)) )
  (  36  ((30 k)) )
  (  37  ((j 31)) )
  (  38  ((26) (27)) )
  (  39  ((i) (h)) )
  (  40  ((38 39)) )
  (  41  ((24) (25)) )
  (  42  ((24) (28)) )
  (  43  ((41 42)) )
  (  44  ((27) (i)) )
  (  45  ((22) (23)) )
  (  46  ((22) (28)) )
  (  47  ((45 46)) )
  (  48  ((h) (26)) )
  (  49  ((20) (21)) )
```

```
(   50   ((49 19)) )
(   51   ((21) (18)) )
(   52   ((51 17)) )
(   53   ((16) (21)) )
(   54   ((15) (f)) )
(   55   ((g) (14)) )
(   56   ((54 55)) )
(   57   ((13 12)) )
(   58   ((14 g)) )
(   59   ((f 15)) )
(   60   ((10) (11)) )
(   61   ((e) (d)) )
(   62   ((60 61)) )
(   63   ((8) (9)) )
(   64   ((8) (12)) )
(   65   ((63 64)) )
(   66   ((11) (e)) )
(   67   ((6) (7)) )
(   68   ((6) (12)) )
(   69   ((67 68)) )
(   70   ((d) (10)) )
(   71   ((4) (5)) )
(   72   ((71 3)) )
(   73   ((2) (5)) )
(   74   ((1) (5)) )
(   75   ((74 0)) ) ))
```

*Form 2:* remove inverters

```
((cm85a)
 ((a unk)(b unk)(c unk)(d unk)(e unk)(f unk)
  (g unk)(h unk)(i unk)(j unk)(k unk))
 ((oa 75)(ob 73)(oc 72))
 ((  34  (((36) (37))) )
  (  35  (((40) (53))) )
  (  36  ((k (j))) )
  (  37  ((j (k))) )
  (  38  (h i) )
  (  39  ((h) (i)) )
  (  40  ((38 39)) )
  (  41  (44 50) )
  (  42  (50 53) )
  (  43  ((41 42)) )
  (  44  (h (i)) )
  (  45  (48 52) )
  (  46  (52 53) )
  (  47  ((45 46)) )
  (  48  (i (h)) )
  (  49  (57 59) )
  (  50  ((49 (65))) )
  (  51  (57 58) )
  (  52  ((51 (69))) )
  (  53  (56 57) )
  (  56  (((58) (59))) )
  (  57  (((62) (b))) )
  (  58  ((g (f))) )
  (  59  ((f (g))) )
  (  60  (d e) )
  (  61  ((d) (e)) )
  (  62  ((60 61)) )
  (  63  (66 a) )
  (  64  (a b) )
  (  65  ((63 64)) )
  (  66  (d (e)) )
  (  67  (70 c) )
  (  68  (b c) )
  (  69  ((67 68)) )
  (  70  (e (d)) )
  (  71  (35 36) )
  (  72  ((71 (47))) )
  (  73  (34 35) )
  (  74  (35 37) )
  (  75  ((74 (43))) )  ))
```

***Form 3:*** remove single referenced cells

```
((cm85a)
 ((a unk)(b unk)(c unk)(d unk)(e unk)(f unk)
  (g unk)(h unk)(i unk)(j unk)(k unk))
 ((oa 75)(ob 73)(oc 72))
 ((  35  (( (53) (h (i)) (i (h)) )) )
  (  36  ((k (j))) )
  (  37  ((j (k))) )
  (  50  (( (57 59) ((a b) (a (d (e)))))) )
  (  52  (( (57 58) ((b c) (c (e (d)))))) )
  (  53  (57 (58) (59)) )
  (  57  (( (b) (d (e)) (e (d)) )) )
  (  58  ((g (f))) )
  (  59  ((f (g))) )
  (  72  (( (35 36) ((52 53) (52 (i (h)))) )) )
  (  73  (35 (36) (37)) )
  (  75  (( (35 37) ((50 53) (50 (h (i)))) )) )
 ))
```

***Form 4:*** abstract equality parts

```
Z = (h (i))
Y = (i (h))
W = (d (e))
V = (e (d))
T = (k (j))
S = (j (k))
R = (g (f))
P = (f (g))

 ((  35  (((53) Z Y)) )
  (  50  (((57 (P)) ((a b) (a W)))) )
  (  52  (((57 (R)) ((c b) (c V)))) )
  (  53  (57 R P) )
  (  57  (((b) W V)) )
  (  72  (((35 (T)) ((52 53) (52 Y)))) )
  (  73  (35 T S) )
  (  75  (((35 (S)) ((50 53) (50 Z)))) )
 ))
```

***Form 5:*** distribute

```
 ((  35  (((53) Z Y)) )
  (  50  ((a (57 (P)) ((b) (W)))) )
  (  52  ((c (57 (R)) ((b) (V)))) )
  (  53  (57 R P) )
  (  57  (((b) W V)) )
  (  72  ((52 (35 (T)) ((53) (Y)))) )
  (  73  (35 T S) )
  (  75  ((50 (35 (S)) ((53) (Z)))) )
 ))
```

***Form 6:*** expand out all cells

```
 ((  72  (( c ((b) (V (W (R (P (Y (Z (T)))))))) )) )       out-1
  (  73  ((b) W V R P Z Y T S) )                           out-3
  (  75  (( a ((b) (W (V (P (R (Z (Y (S)))))))) )) )      out-2

Z = (h (i))
Y = (i (h))
W = (d (e))
V = (e (d))
T = (k (j))
S = (j (k))
R = (g (f))
P = (f (g))
```

***Form 7:*** construct LUT

```
 ((  72  (( c ((b) (V (W (R (P (Y (Z (T)))))))) )) )
  (  73  ((b) W V R P Z Y T S) )
  (  75  (( a ((b) (W (V (P (R (Z (Y (S)))))))) )) )

 ((  72  7 )
  (  73  11 )
  (  75  8 ))

 1= (Y (Z (T)))
 2= (Z (Y (S)))
 3= (R (P 1))          3-var
 4= (P (R 2))          3-var
 5= ((b) (V (W 3)))
 6= ((b) (W (V 4)))
 7= (( c 5 ))          2-var
 8= (( a 6 ))          2-var
 9= Z Y W V
10= R P T S
11= ((b) 9 10)         3-var

Z = (h (i))
Y = (i (h))
W = (d (e))
V = (e (d))
T = (k (j))
S = (j (k))
R = (g (f))
P = (f (g))


 ((  72  (( c ((b) (V (W (R (P 1)))))) )) )
  (  73  11 )
  (  75  (( a ((b) (W (V (P (R 2)))))) )) )

 1= (Y (Z (T)))
 2= (Z (Y (S)))
 9= Z Y W V
10= R P T S
11= ((b) 9 10)         3-var
```